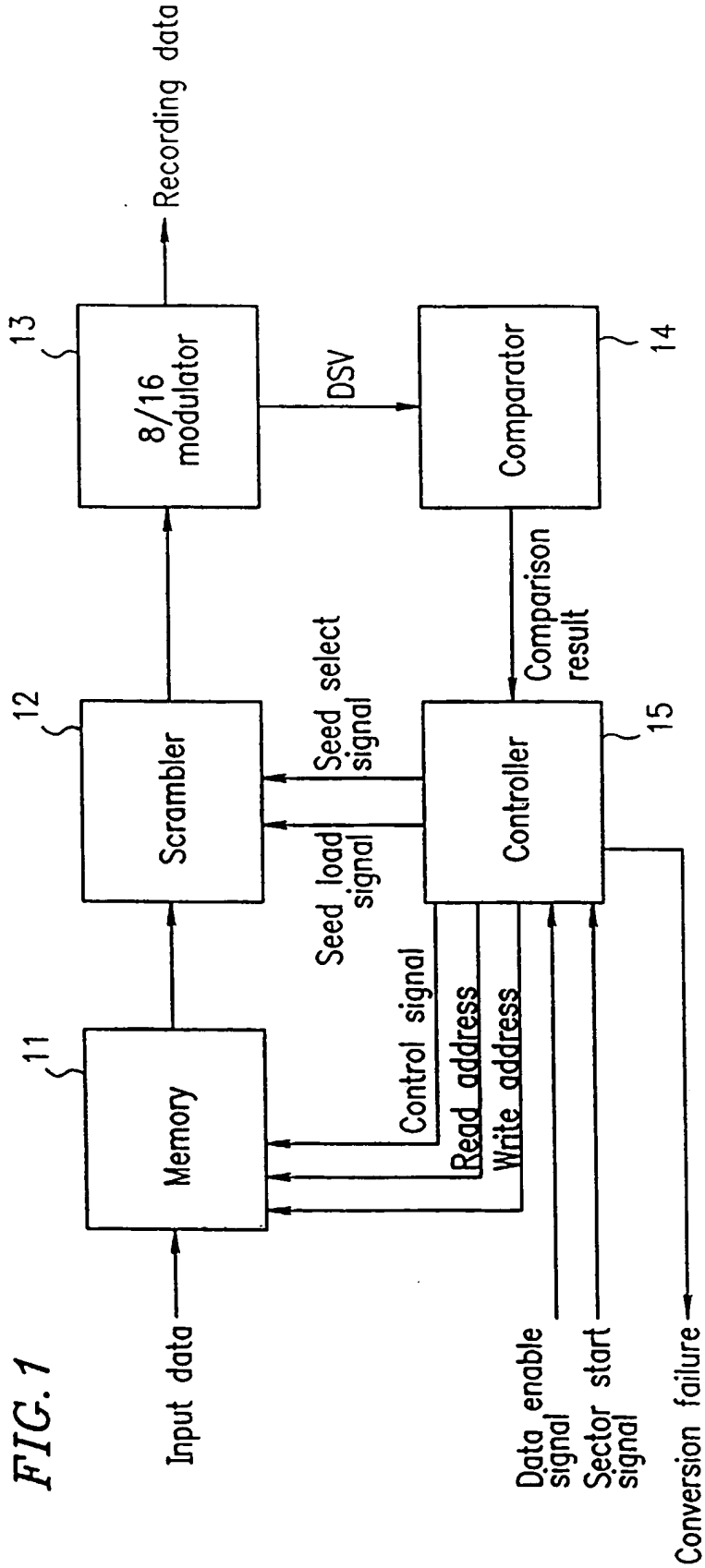

Recording data
13
8/16 modulator
DSV
Comparator
14
Comparison result
12
Scrambler
Seed select signal
Seed load signal
Controller
15
Control signal
Read address
Write address
11
Memory
Input data
Data enable signal
Sector start signal
Conversion failure signal

FIG. 1

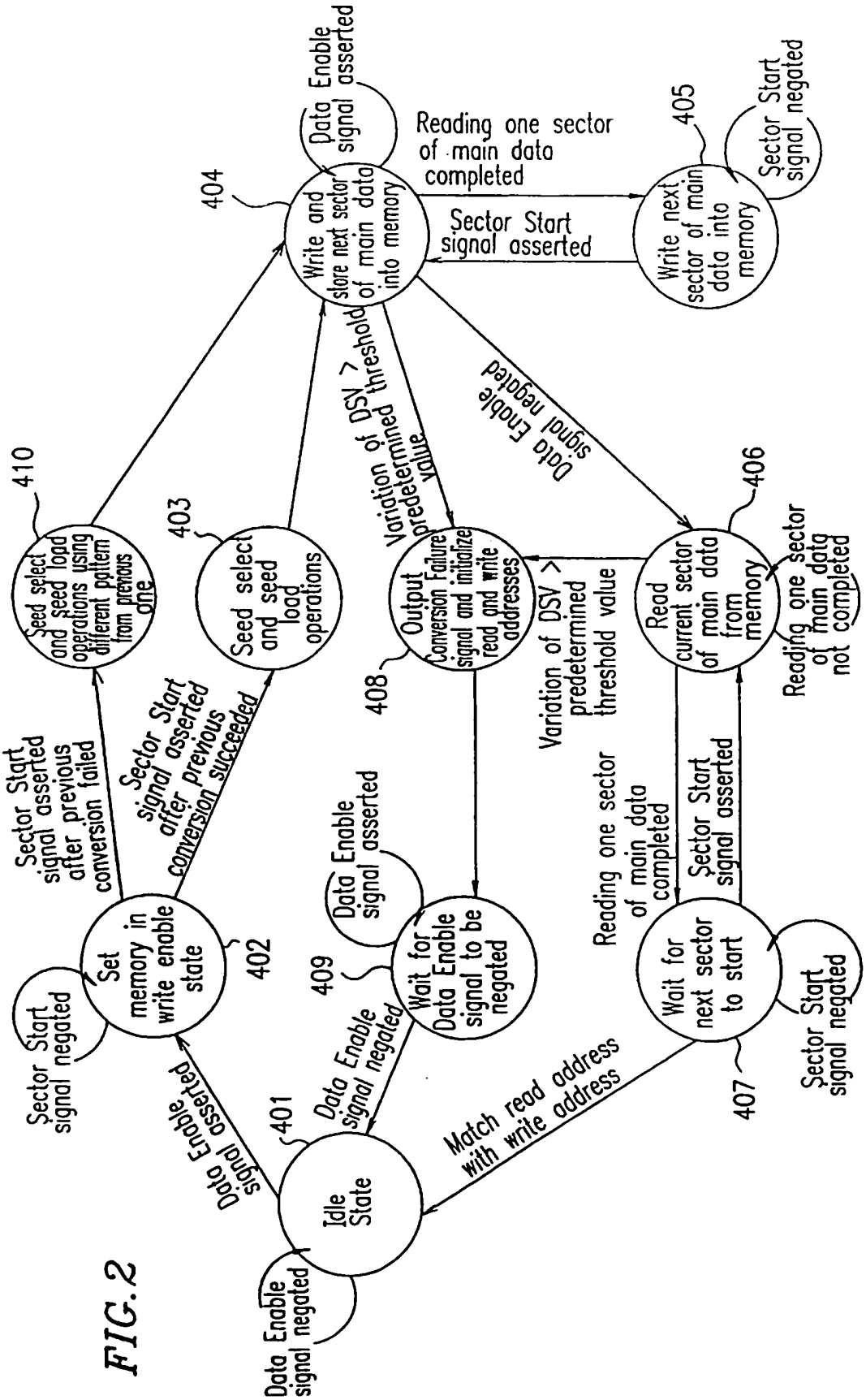

Idle State
401
Set memory in write enable state
402
Seed select and seed load operations
403
Write and store next sector of main data into memory
404
Write next sector of main data into memory
405
Read current sector of main data from memory
406
Wait for next sector to start
407
Output Conversion Failure signal and initialize read and write addresses
408
Wait for Data Enable signal to be negated
409
Seed select and seed load operations using different pattern from previous one
410
Data Enable signal asserted
Data Enable signal negated
Sector Start signal asserted
Sector Start signal negated
Sector Start signal asserted after previous conversion failed
Sector Start signal asserted after previous conversion succeeded
Reading one sector of main data completed
Reading one sector of main data not completed
Variation of DSV > predetermined threshold value
Data Enable signal negated
Match read address with write address

FIG. 2

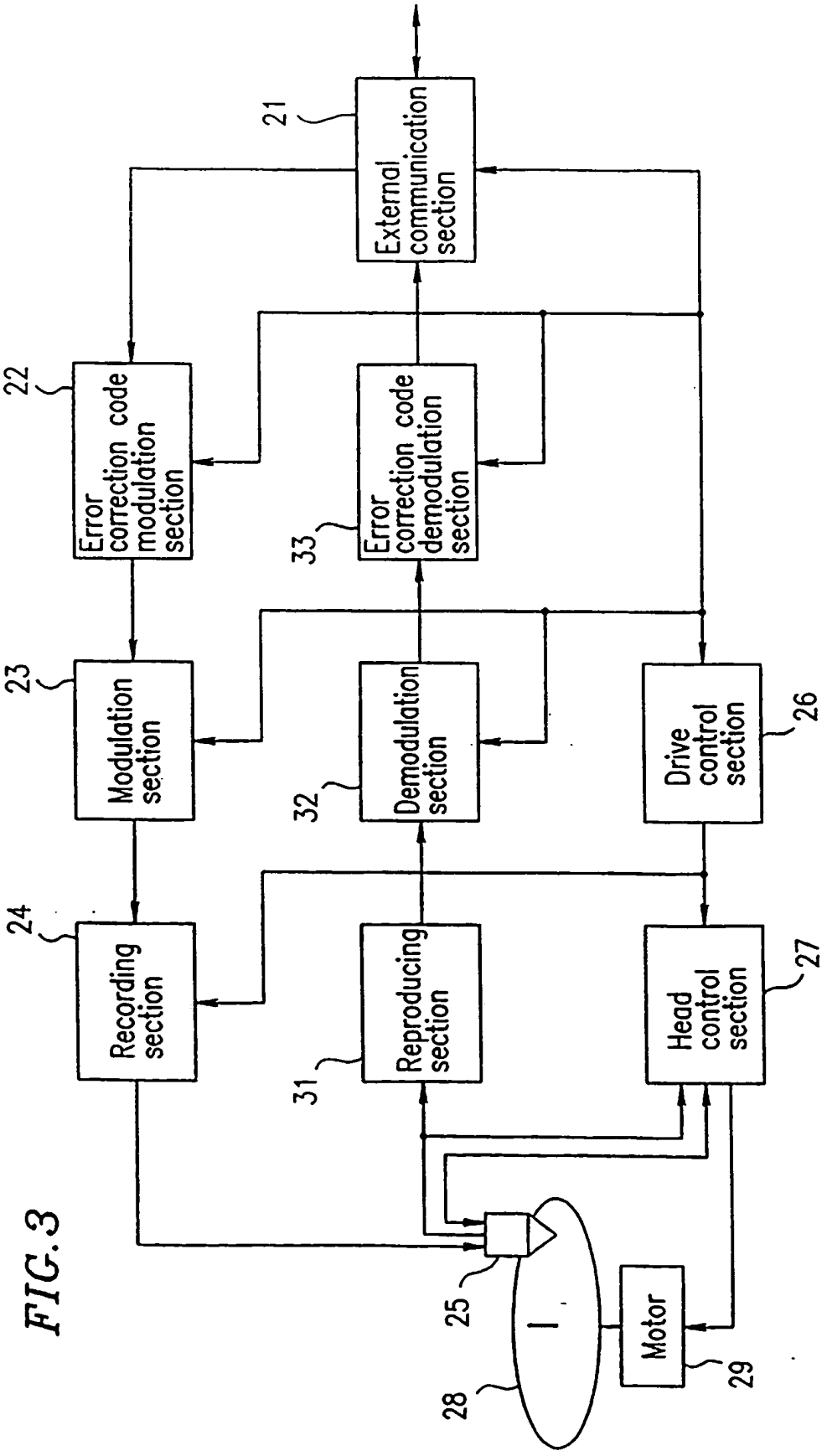

21
External communication section
22
Error correction code modulation section
33
Error correction code demodulation section
23
Modulation section
32
Demodulation section
26
Drive control section
24
Recording section
31
Reproducing section
27
Head control section
25
28
Motor
29

FIG. 3

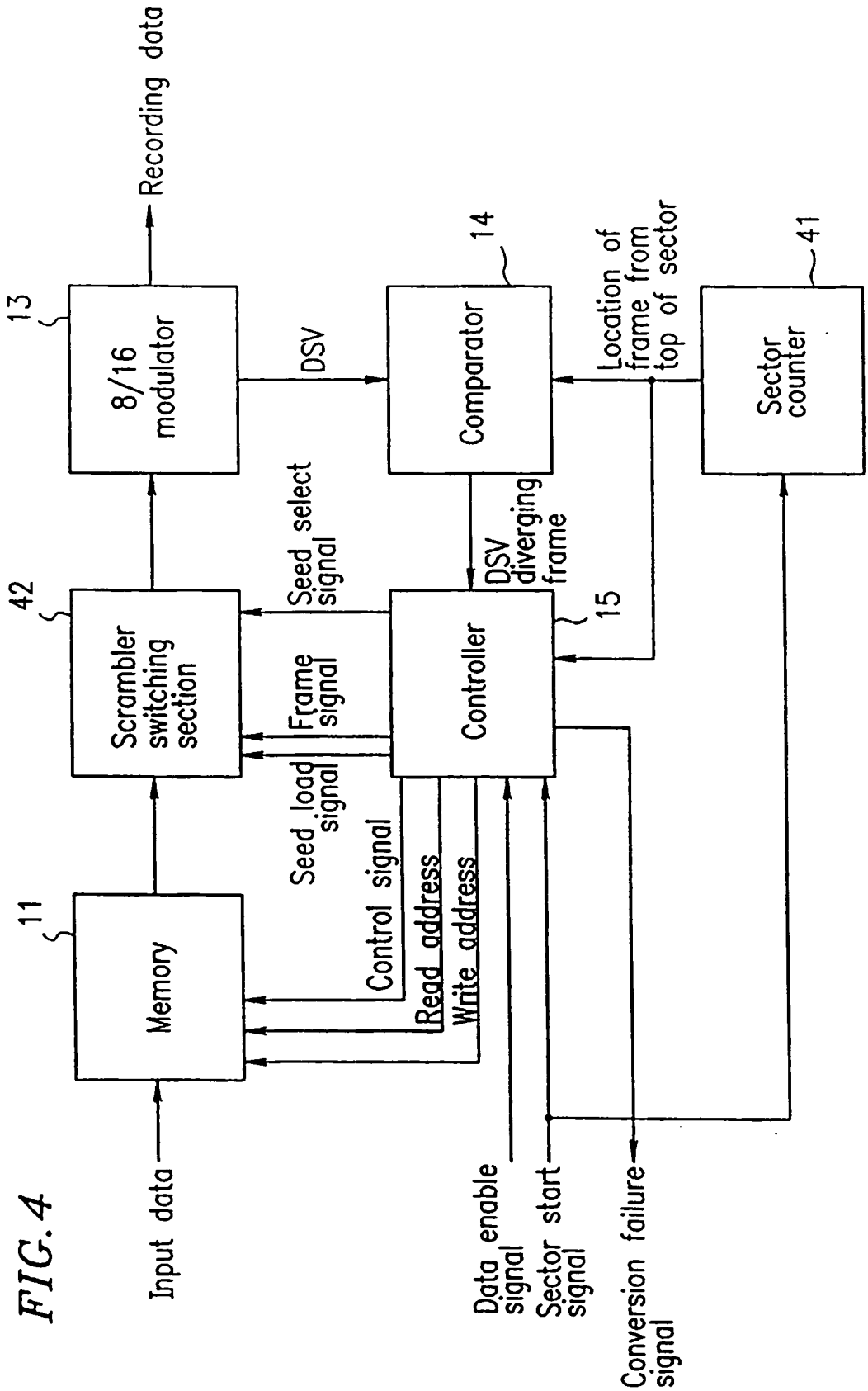

Recording data
13
8/16 modulator
DSV
14
Comparator
Location of frame from top of sector
41
Sector counter
Seed select signal
DSV diverging frame
42
Scrambler switching section
Frame signal
Controller
15
Seed load signal
Control signal
Read address
Write address
11
Memory
Input data
Data enable signal
Sector start signal
Conversion failure signal

FIG. 4

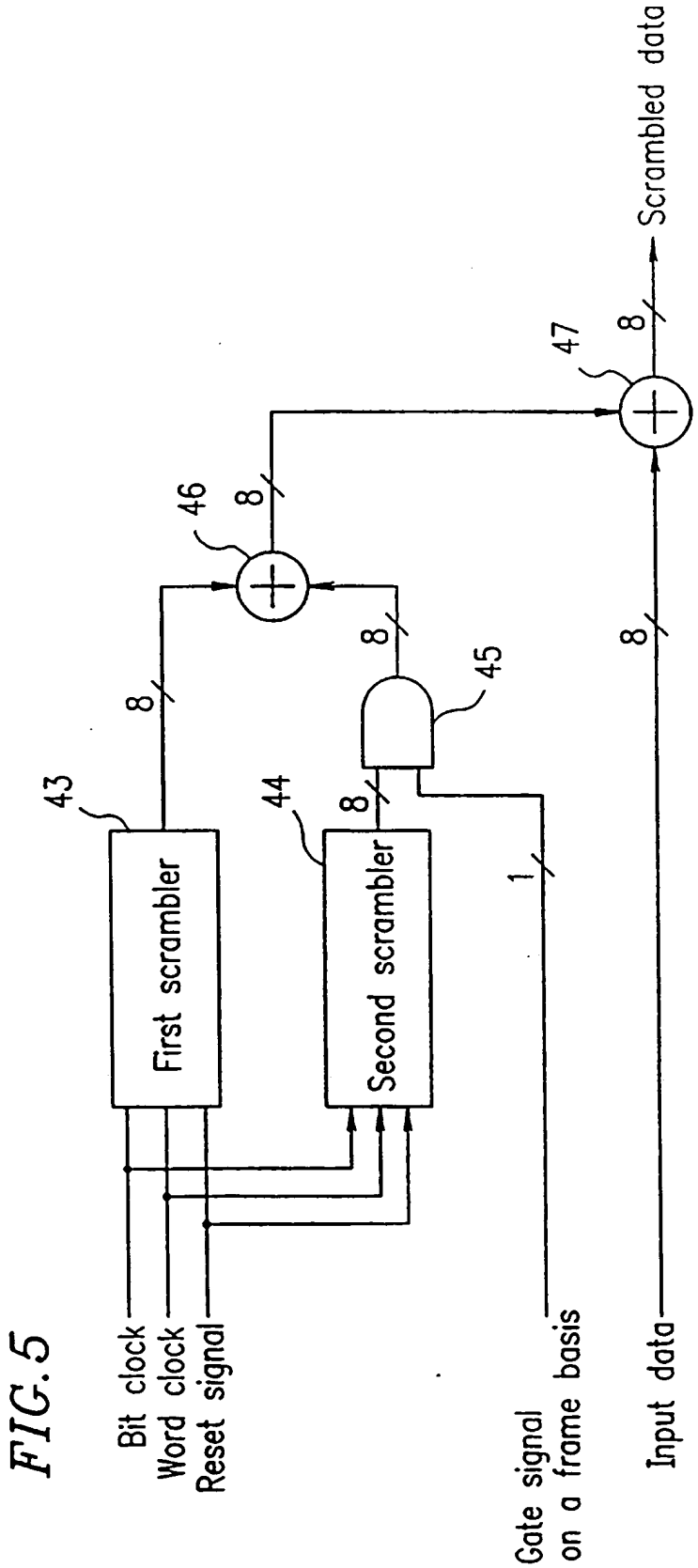

Scrambled data
47
8
46
8
8
45
8
43
44
8
1
First scrambler
Second scrambler
Bit clock
Word clock
Reset signal
Gate signal
on a frame basis
Input data

FIG. 5

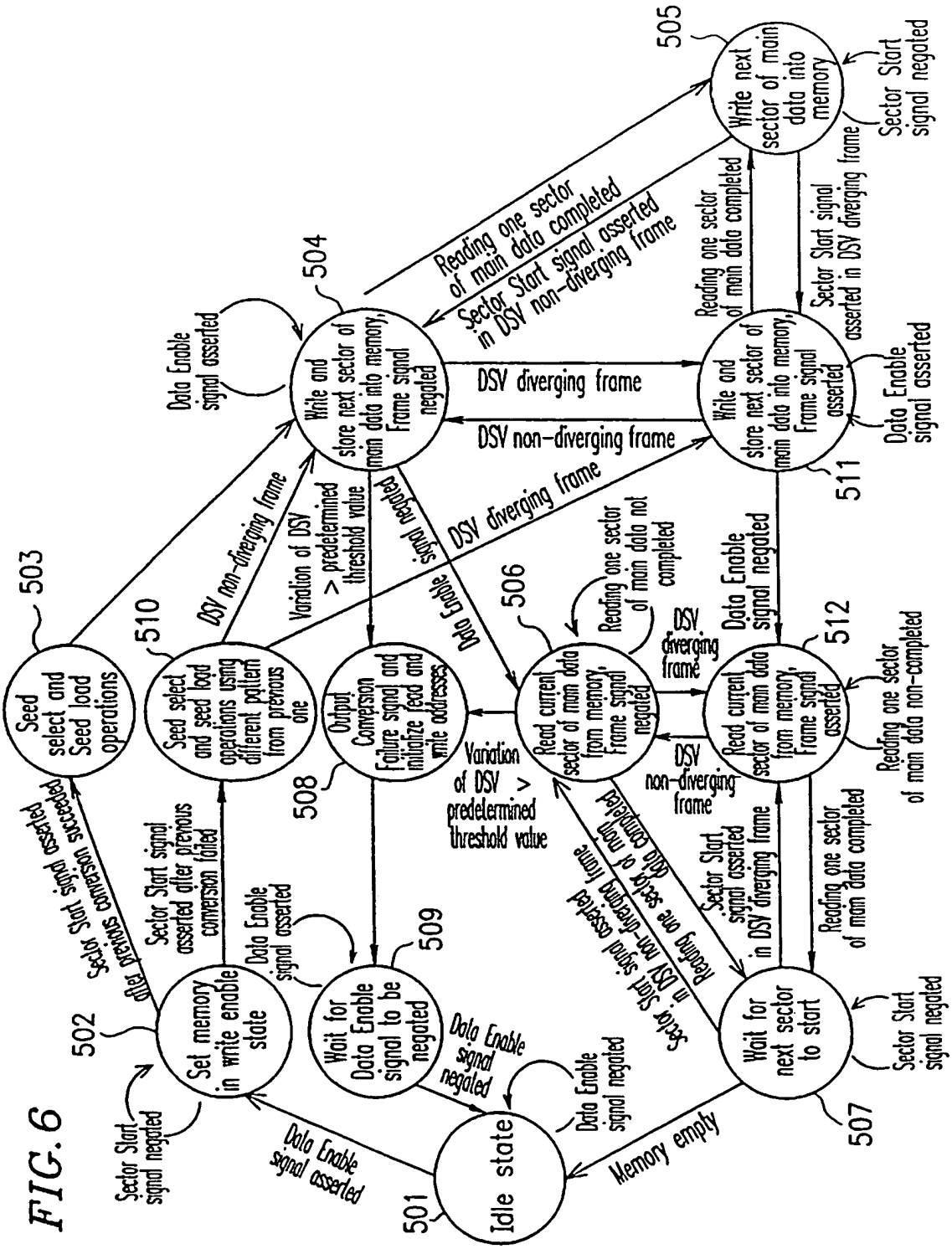

Idle state
501
Set memory in write enable state
502
Seed select and Seed load operations
503
Write and store next sector of main data into memory, Frame signal negated
504
Write next sector of main data into memory
505
Read current sector of main data from memory, Frame signal negated
506
Wait for Data Enable signal to be negated
509
Output Conversion Failure signal and initialize feed and write addresses
508
Seed select and seed load operations using different pattern from previous one
510
Write and store next sector of main data into memory, Frame signal asserted
511
Read current sector of main data from memory, Frame signal asserted
512
Wait for next sector to start
507
Data Enable signal asserted
Sector Start signal asserted after previous conversion failed
Sector Start signal asserted after previous conversion succeeded
Data Enable signal negated
Sector Start signal negated
Memory empty
Reading one sector of main data completed
Sector Start signal asserted in DSV non-diverging frame
Reading one sector of main data completed
Sector Start signal asserted in DSV diverging frame
DSV diverging frame
DSV non-diverging frame
DSV non-diverging frame
DSV diverging frame
Variation of DSV > predetermined threshold value
Variation of DSV > predetermined threshold value
Reading one sector of main data not completed
DSV diverging frame
DSV non-diverging frame
Reading one sector of main data completed
Sector Start signal asserted in DSV diverging frame
Reading one sector of main data non-completed
Reading one sector of main data completed
Sector Start signal negated
Sector Start signal negated
Sector Start signal negated
Sector Start signal negated

FIG. 6

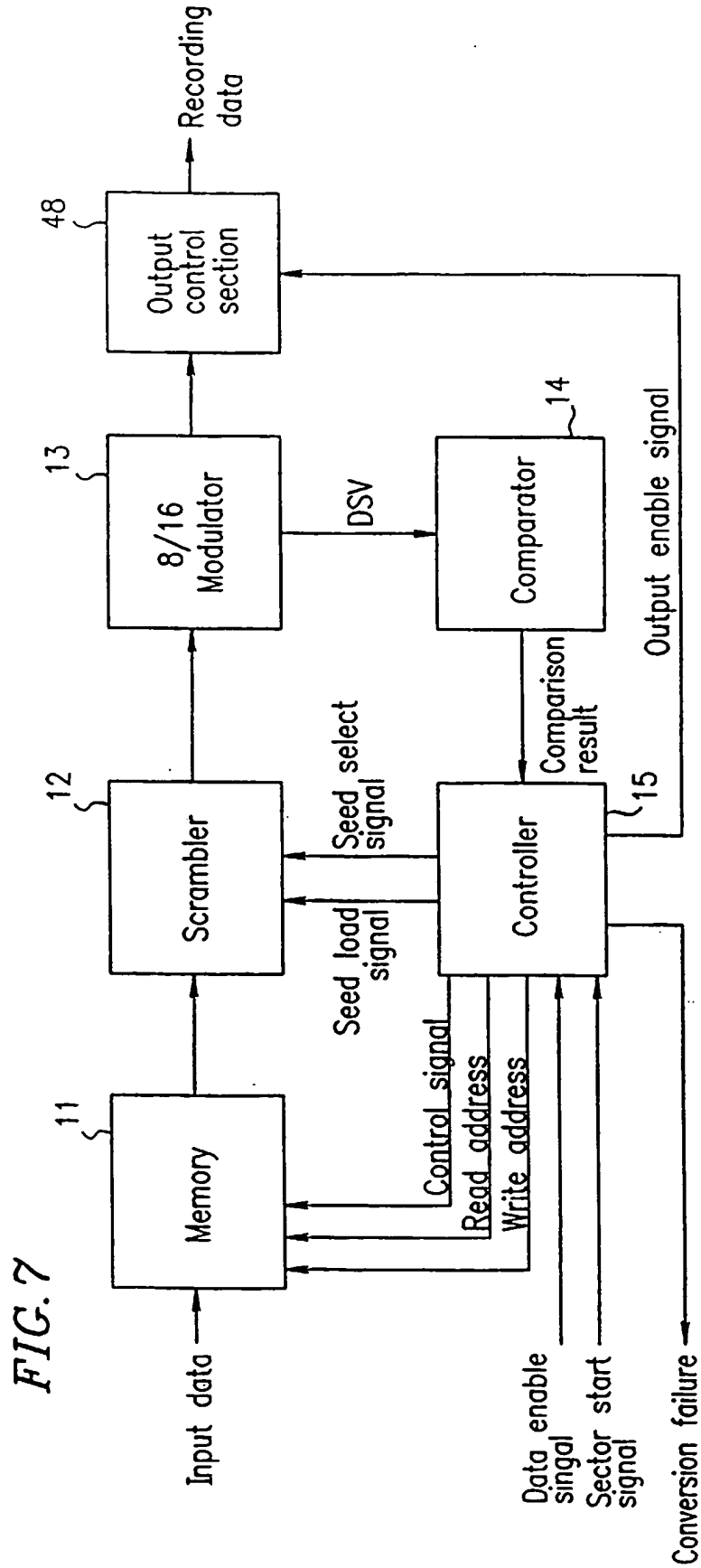

Recording data
48
Output control section
13
8/16 Modulator
DSV
14
Comparator
Output enable signal
12
Scrambler
Seed select signal
Seed load signal
Comparison result
15
Controller
11
Memory
Control signal
Read address
Write address
Input data
Data enable singal
Sector start signal
Conversion failure signal

FIG. 7

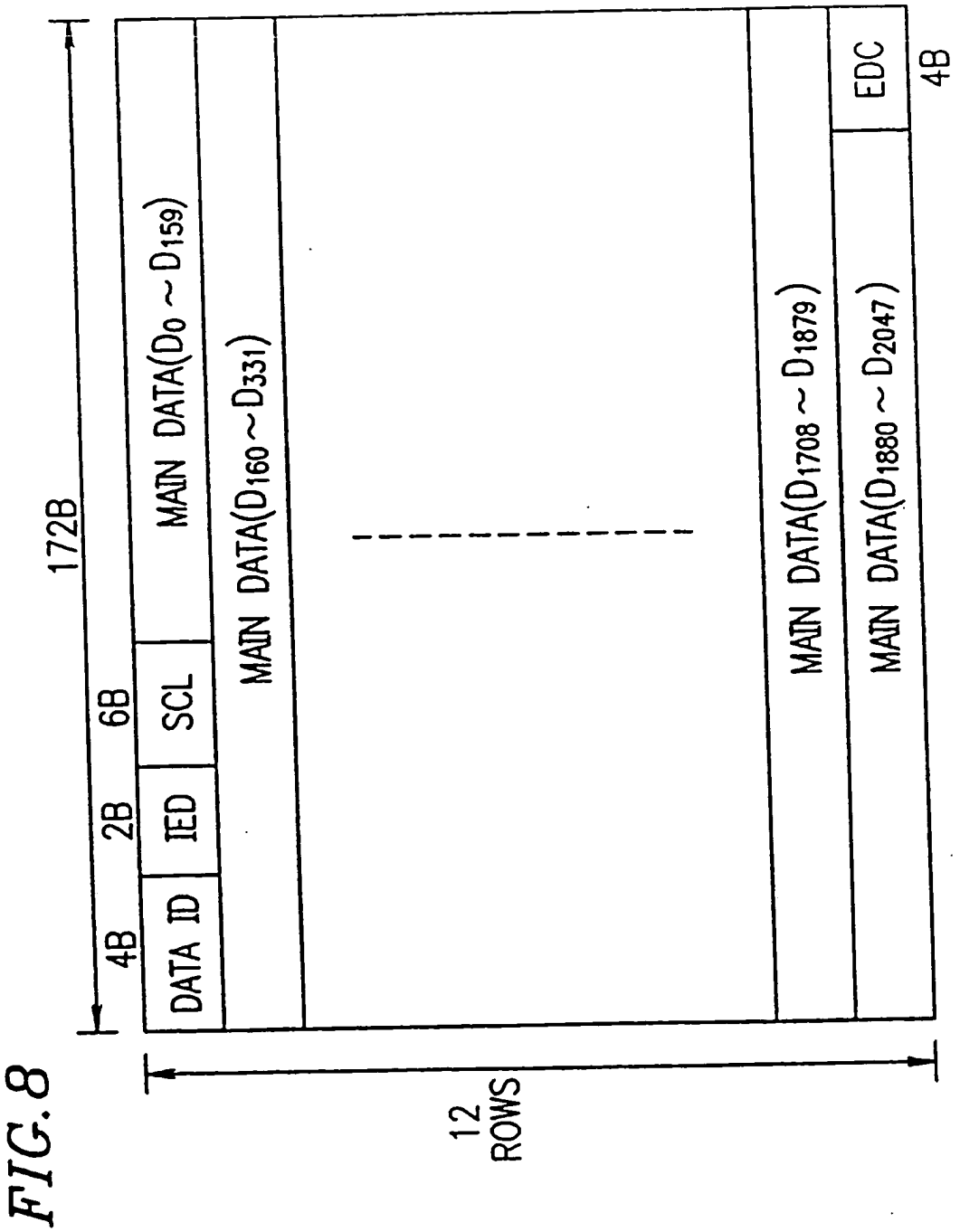

172B
4B
2B
6B
DATA ID
IED
SCL
MAIN DATA(D0 ~ D159)
MAIN DATA(D160 ~ D331)
MAIN DATA(D1708 ~ D1879)
MAIN DATA(D1880 ~ D2047)
EDC
4B
12 ROWS

FIG. 8

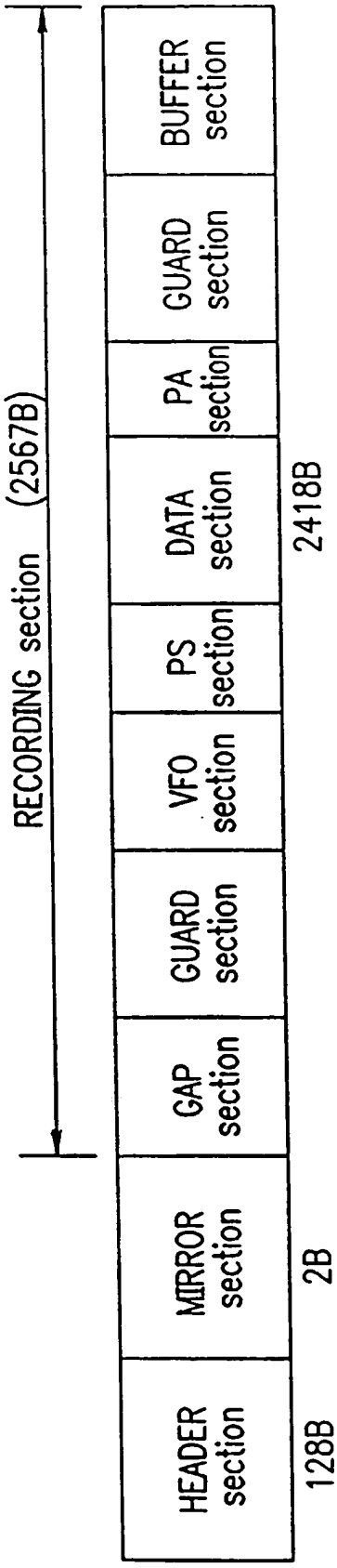

HEADER section
MIRROR section
GAP section
GUARD section
VFO section
PS section
DATA section
PA section
GUARD section
BUFFER section
RECORDING section (2567B)
128B
2B
2418B

FIG. 9

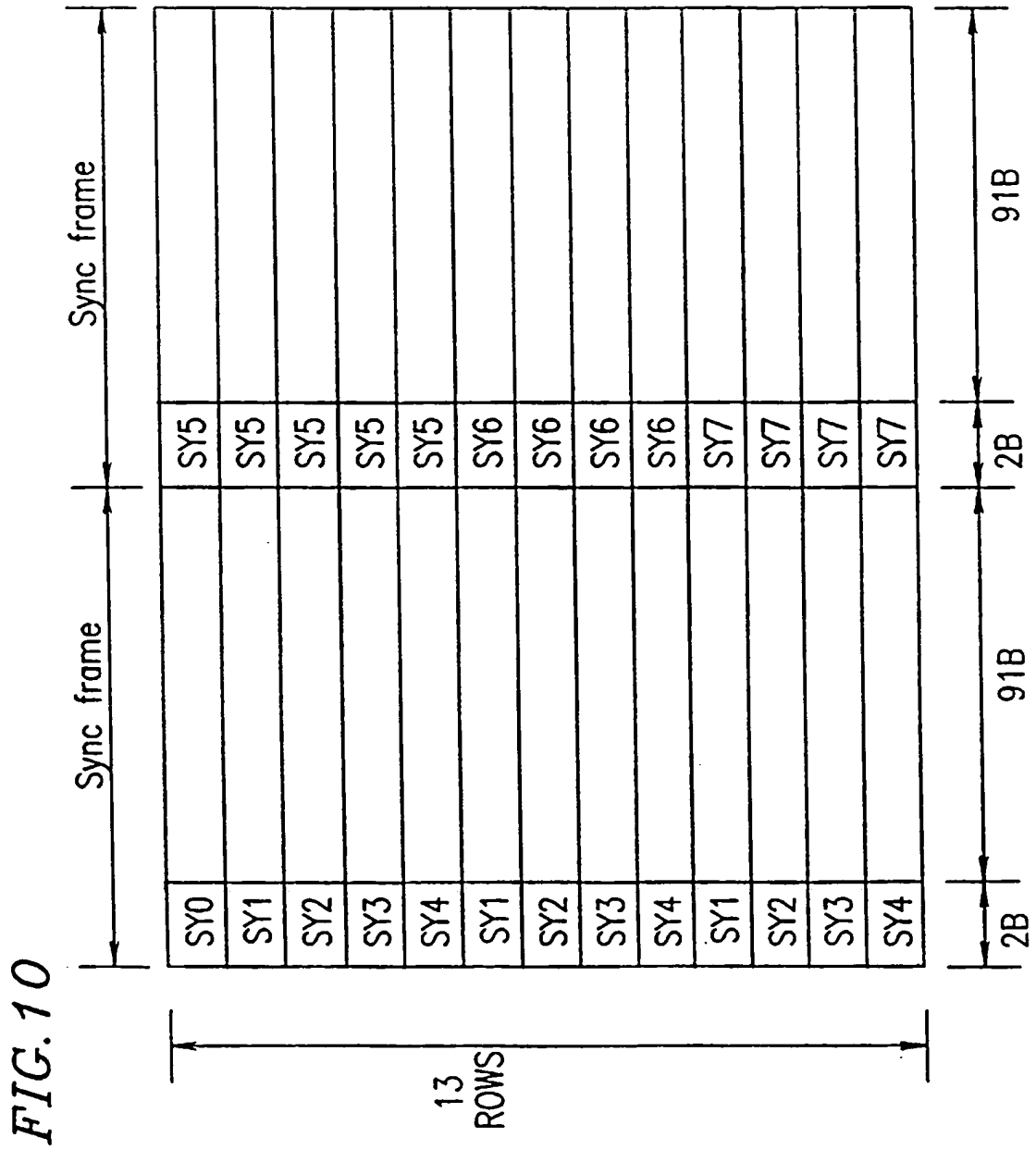
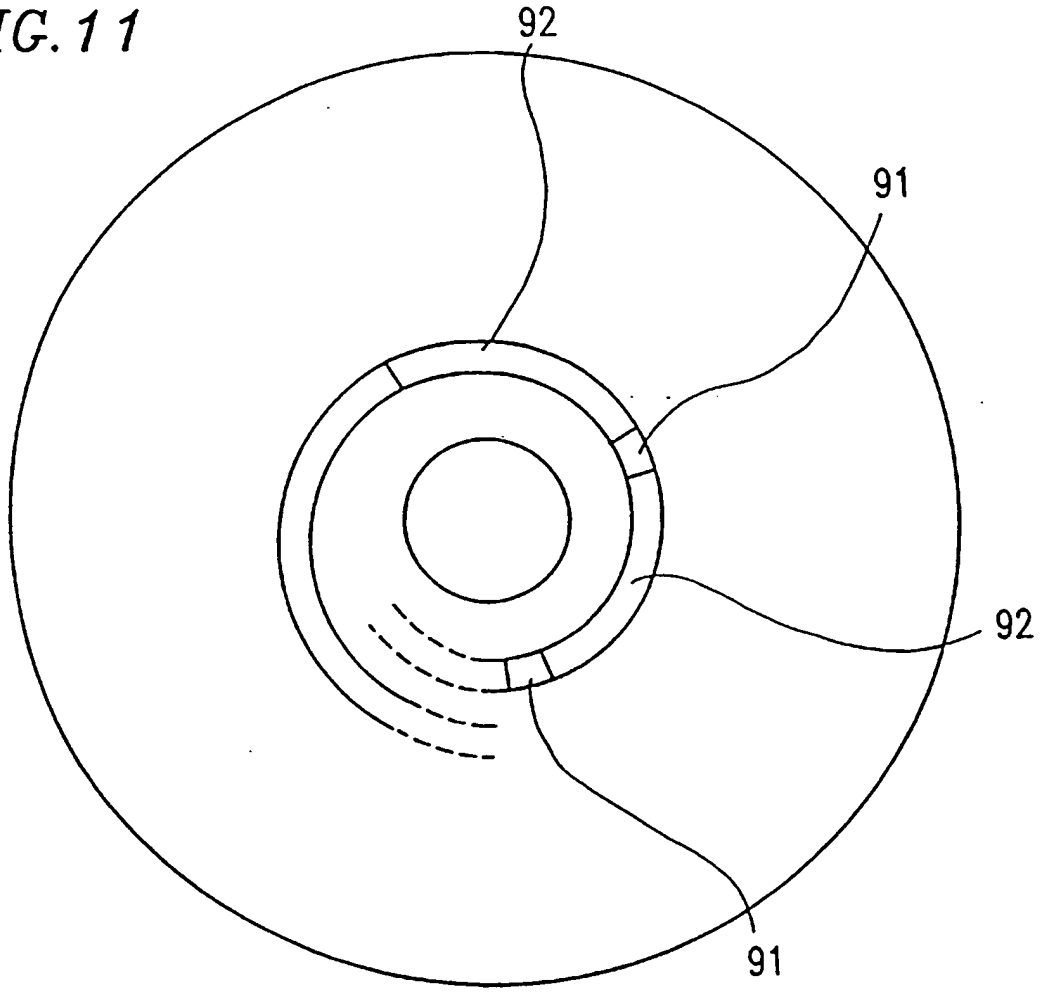

Sync frame
Sync frame
SY0
SY1
SY2
SY3
SY4
SY5
SY6
SY7
91B
2B
91B
2B
13
ROWS

FIG. 10

FIG. 11



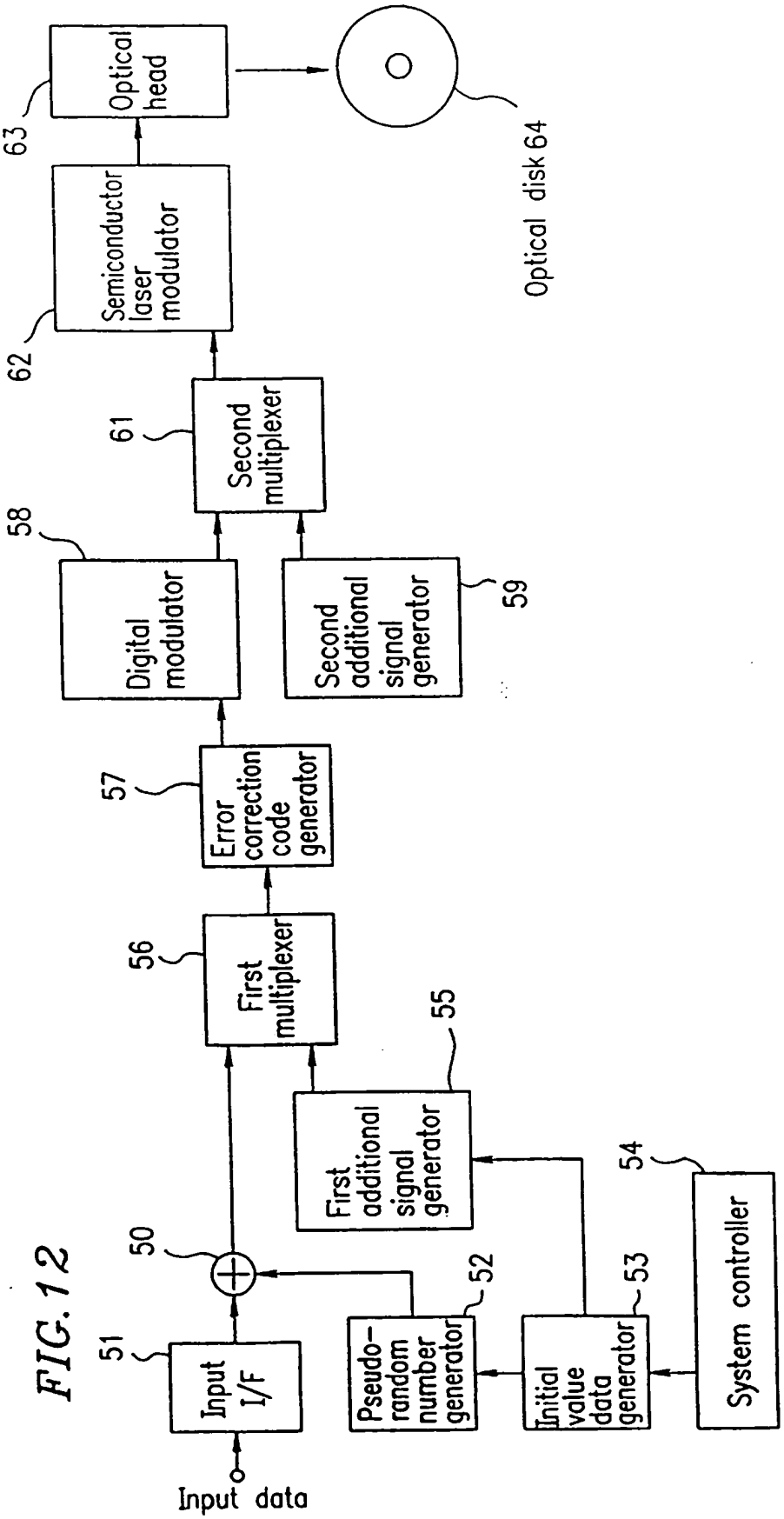

Input data
Input I/F
51
50
Pseudo-random number generator
52
Initial value data generator
53
System controller
54
First additional signal generator
55
First multiplexer
56
Error correction code generator
57
Digital modulator
58
Second additional signal generator
59
Second multiplexer
61
Semiconductor laser modulator
62
Optical head
63
Optical disk 64

FIG. 12

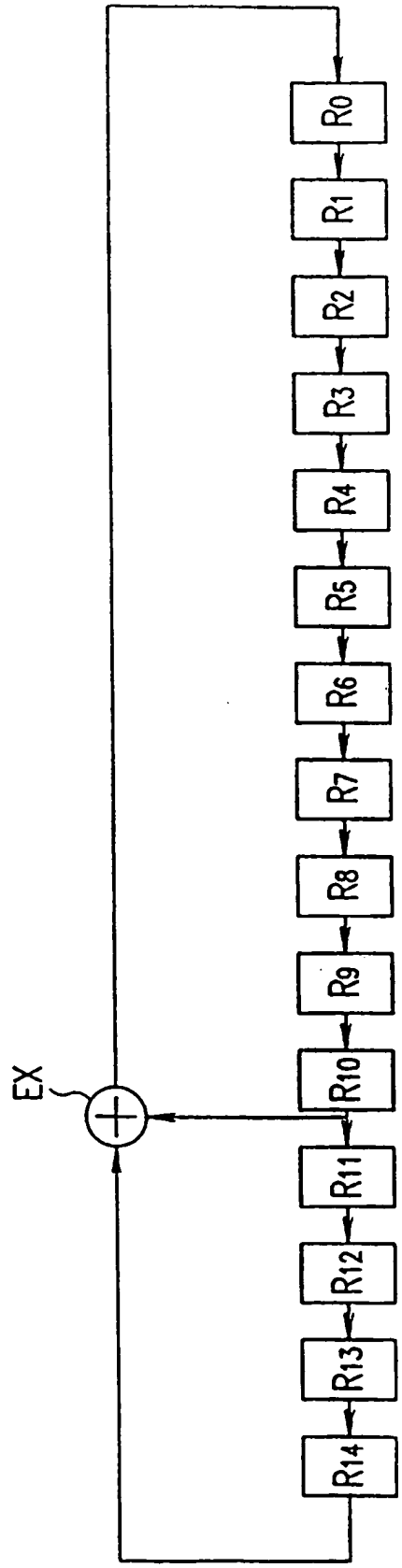


FIG. 13

FIG. 14

Bit string	Initial value
0h	0001h
1	5500
2	0002
3	2A00
4	0004
5	5400
6	0008
7	2800
8	0010
9	5000
A	0020
B	2001
C	0040
D	4002
E	0080
F	0005

FIG. 15

Bit string \ Initial value	Rewrite repetition times 0	Rewrite repetition times 1	Rewrite repetition times 2	-------	Rewrite repetition times 15
0h	0001h	0090h	0003h	-------	0031h
1	5500	3C00	2400	-------	2000
2	0002	00A0	0005	-------	0032
3	2A00	1E00	1200	-------	1600
4	0004	00C0	0006	-------	0034
5	5400	3B00	2300	-------	2B00
6	0008	00F0	0007	-------	0038
7	2800	1D00	1100	-------	1300
8	0010	0009	0030	-------	0013
9	5000	3A00	2500	-------	2A00
A	0020	000A	0050	-------	0023
B	2001	1003	3001	-------	2007
C	0040	0000	0060	-------	0043
D	4002	2006	6002	-------	400E
E	0080	000F	0070	-------	0083
F	0005	00A3	0052	-------	00A2

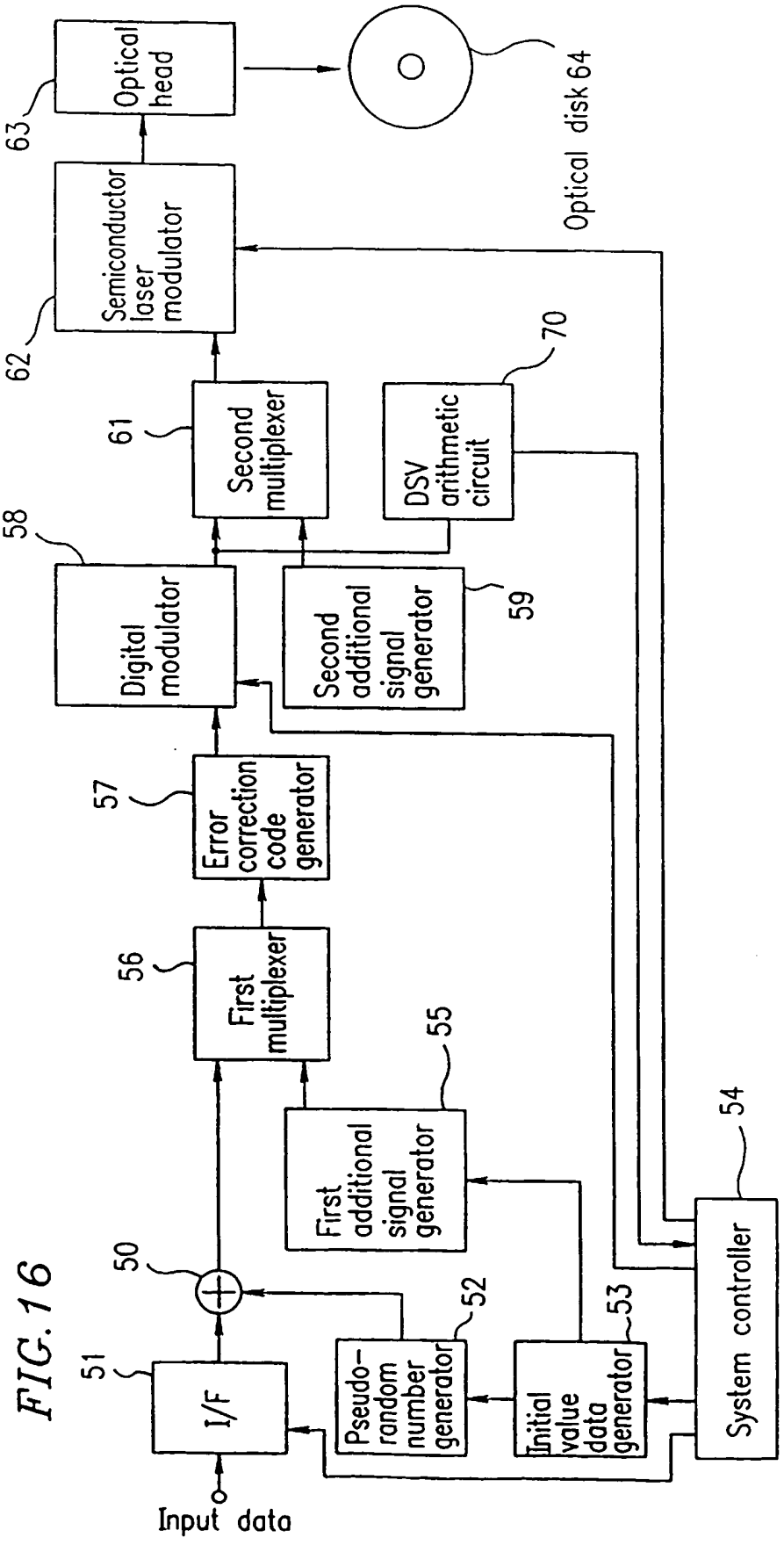

Input data
I/F
51
50
Pseudo-random number generator
52
Initial value data generator
53
System controller
54
First additional signal generator
55
First multiplexer
56
Error correction code generator
57
Digital modulator
58
Second additional signal generator
59
DSV arithmetic circuit
70
Second multiplexer
61
Semiconductor laser modulator
62
Optical head
63
Optical disk 64

FIG. 16

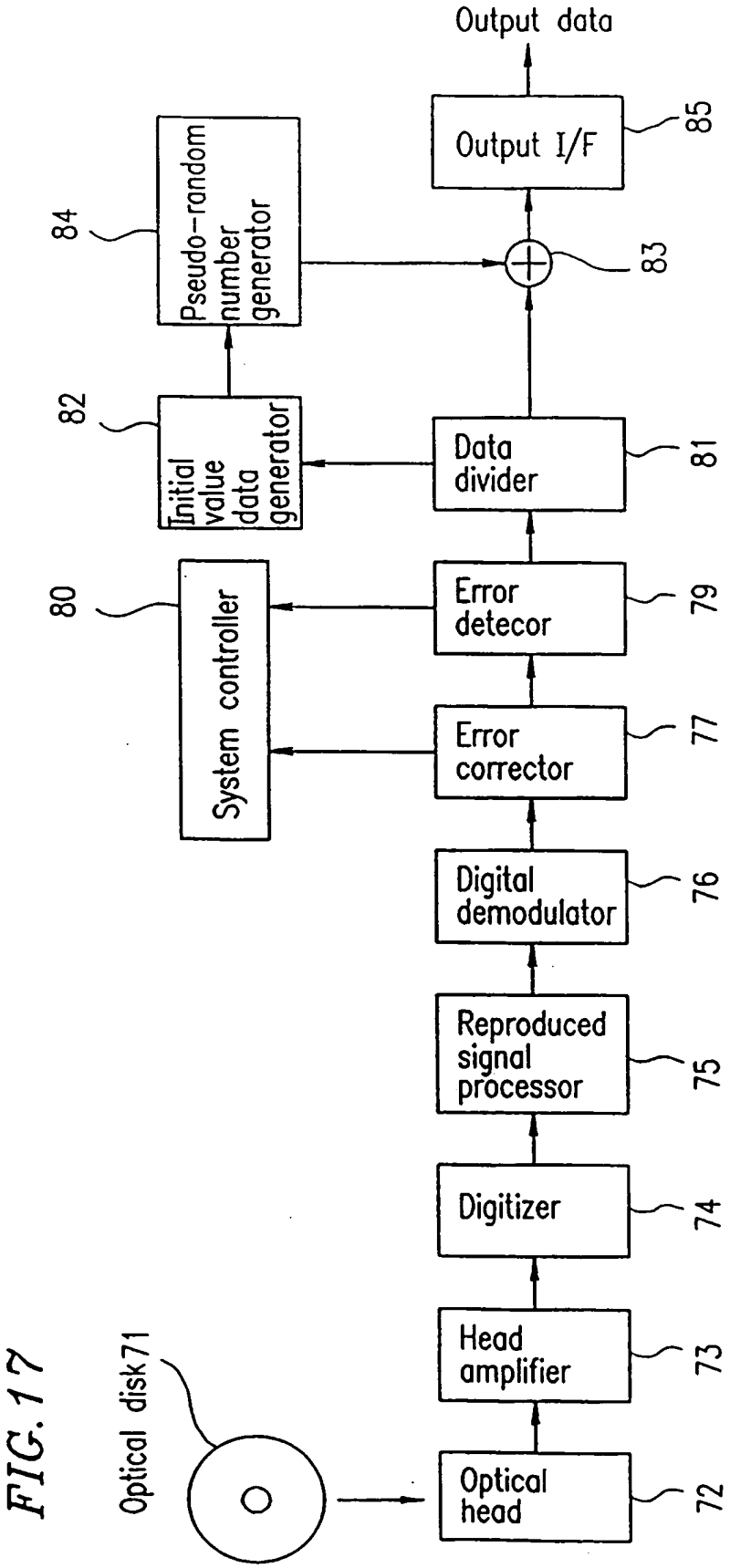

Output data
Output I/F
85
Pseudo-random number generator
84
83
Initial value data generator
82
Data divider
81
System controller
80
Error detecor
79
Error corrector
77
Digital demodulator
76
Reproduced signal processor
75
Digitizer
74
Head amplifier
73
Optical disk 71
Optical head
72

FIG. 17

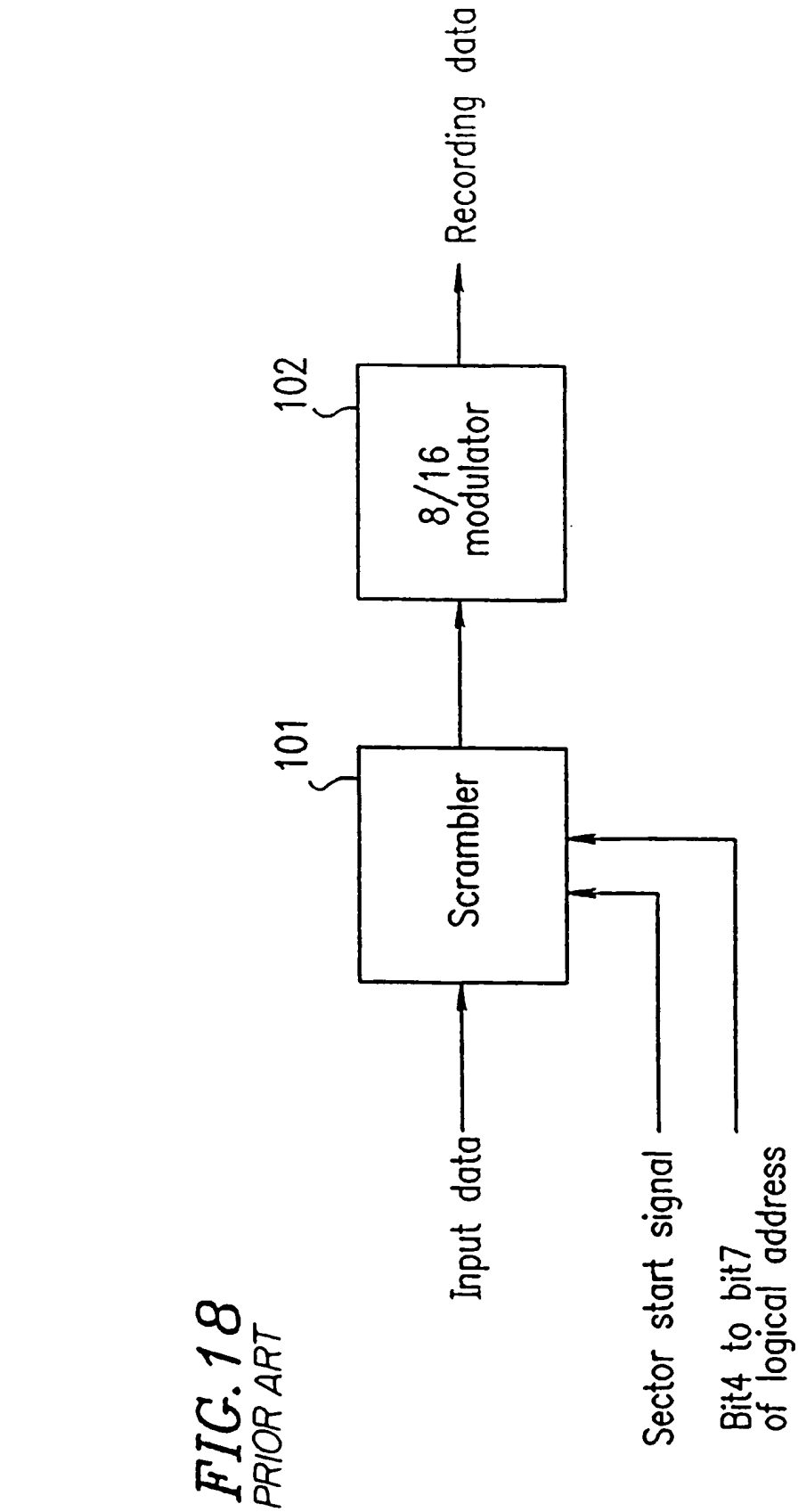


FIG. 18
PRIOR ART

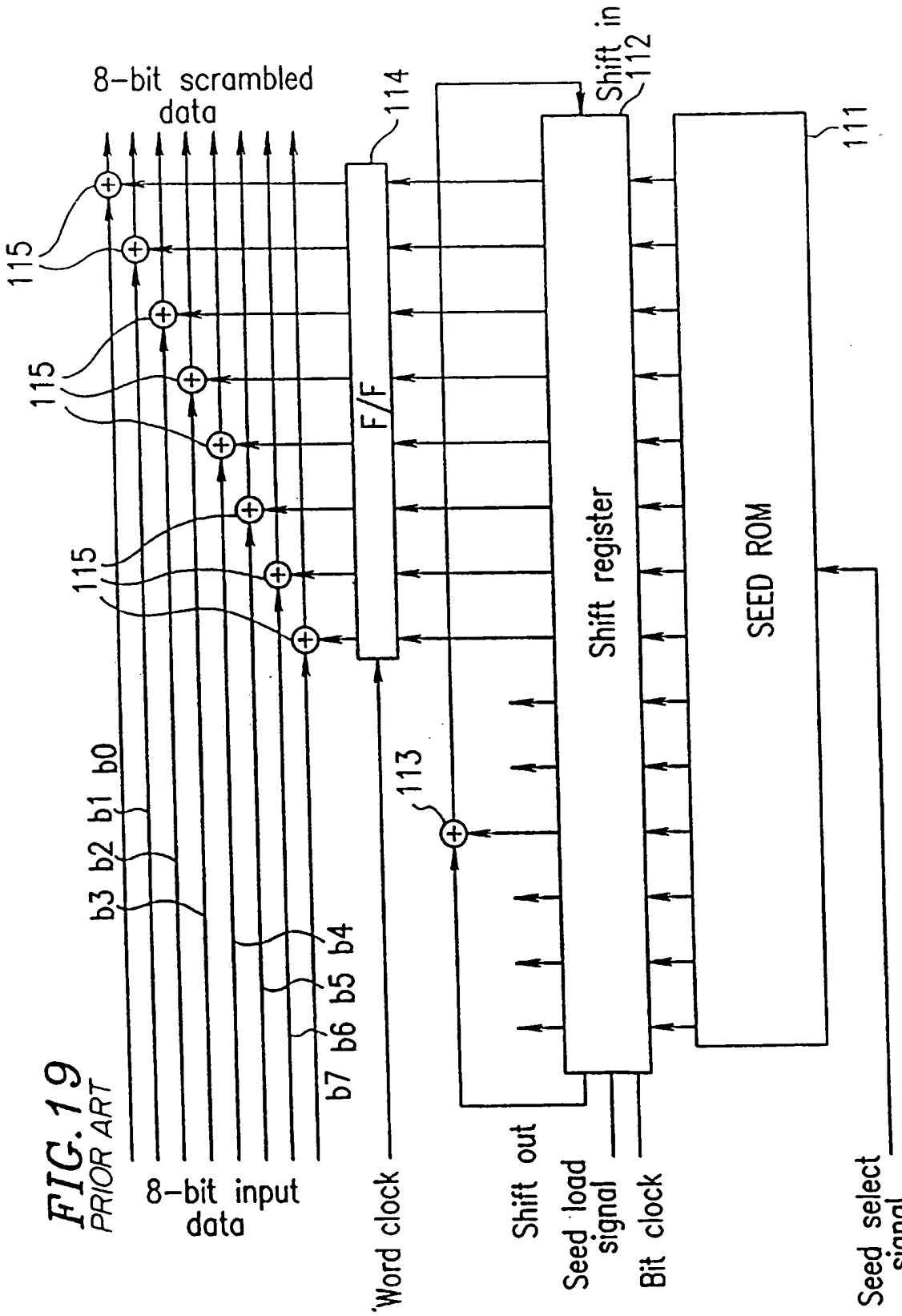


FIG. 19
PRIOR ART

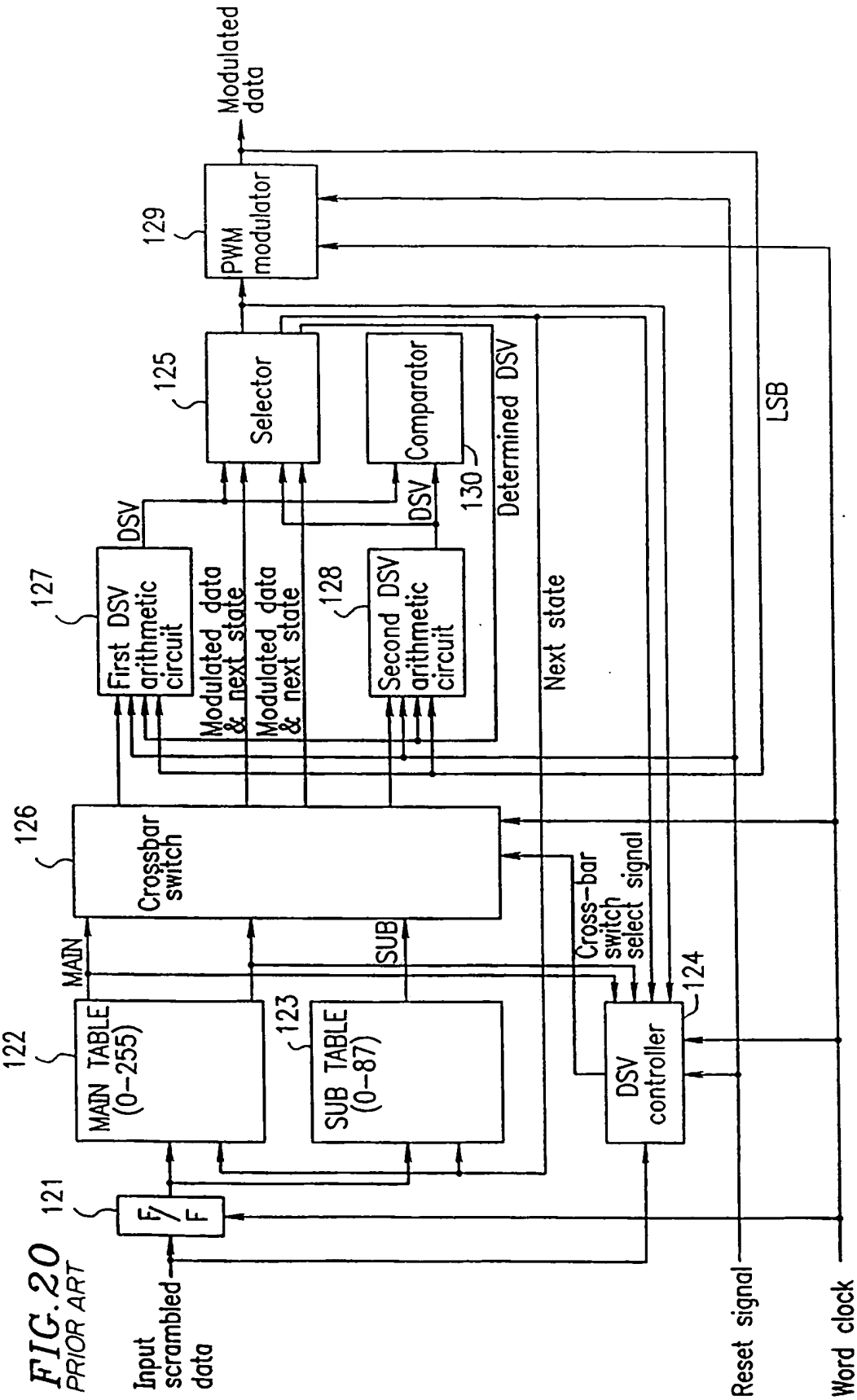


FIG. 20
PRIOR ART

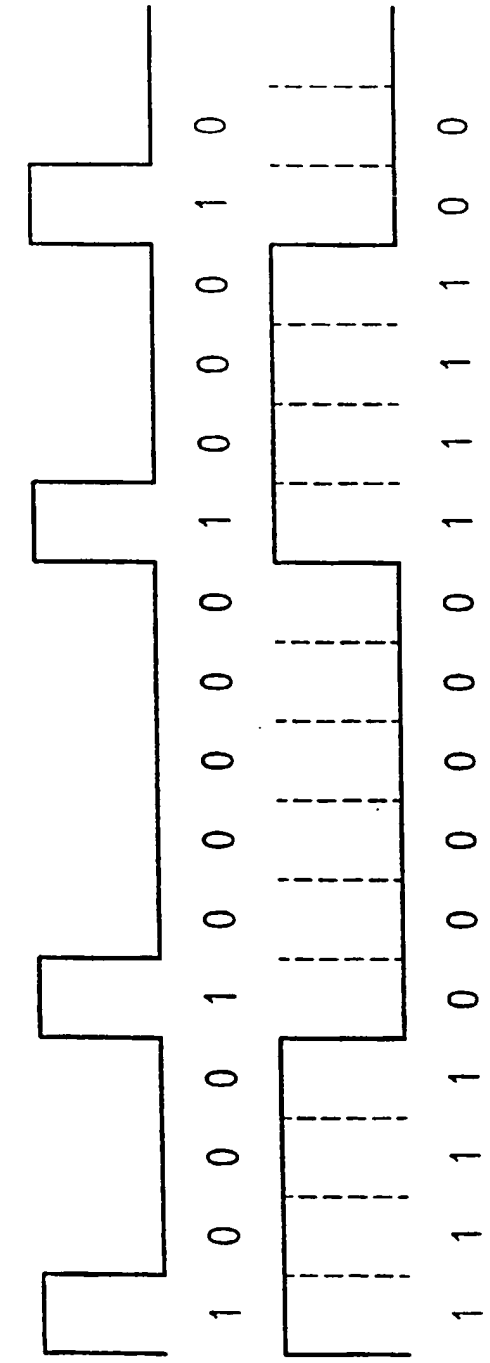


FIG.21A
PRIOR ART

FIG.21B
PRIOR ART

FIG. 22
PRIOR ART

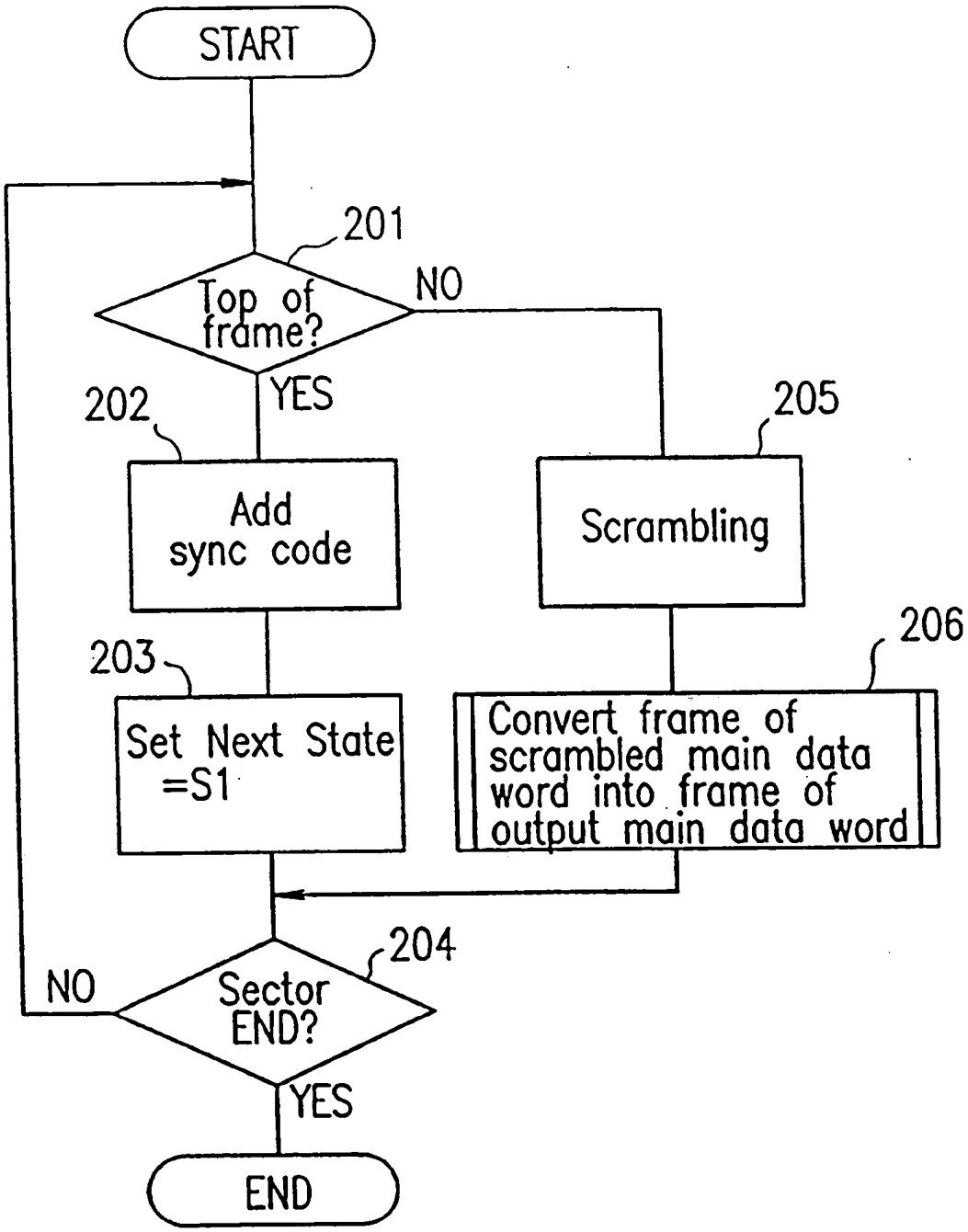


FIG. 23
PRIOR ART

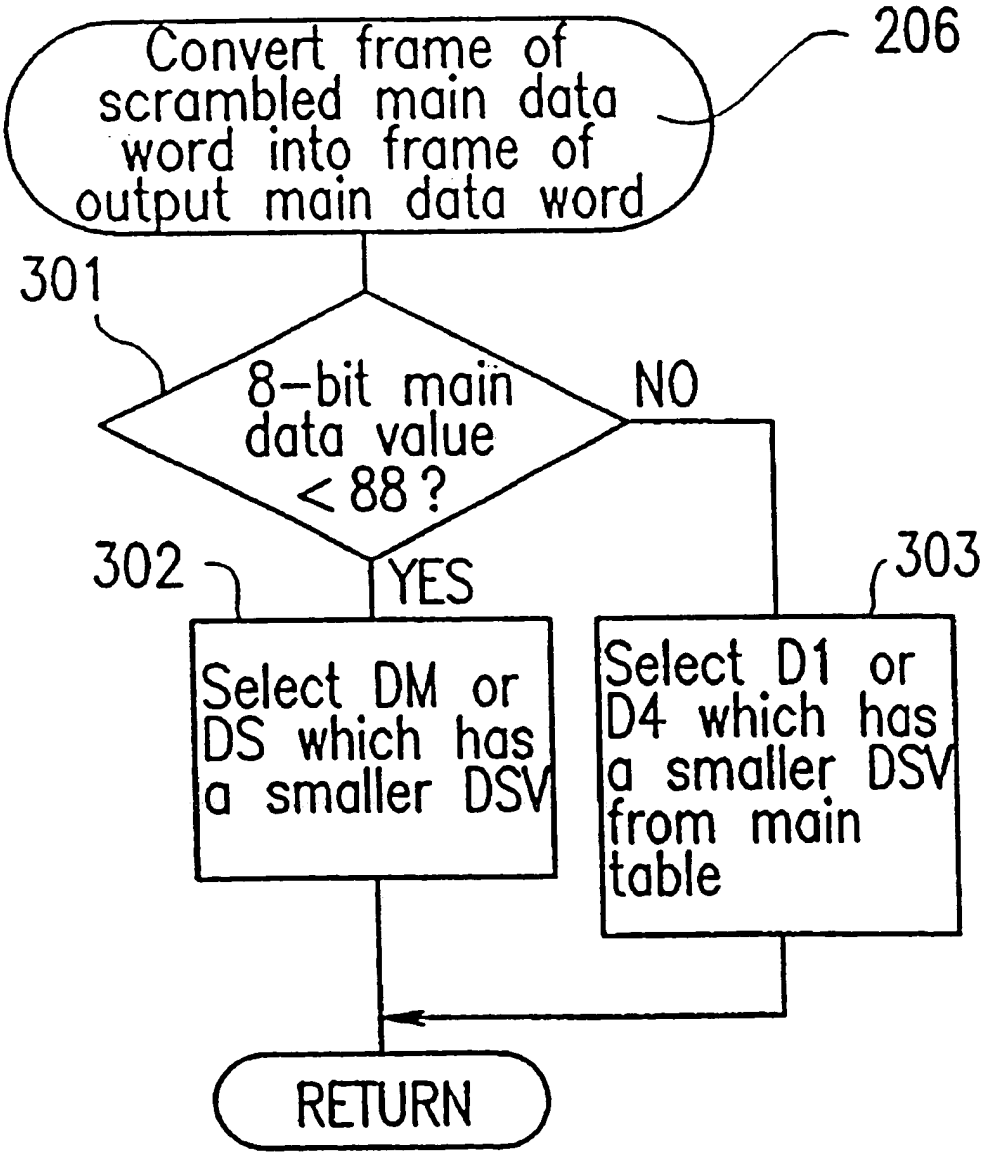


FIG. 24A
PRIOR ART

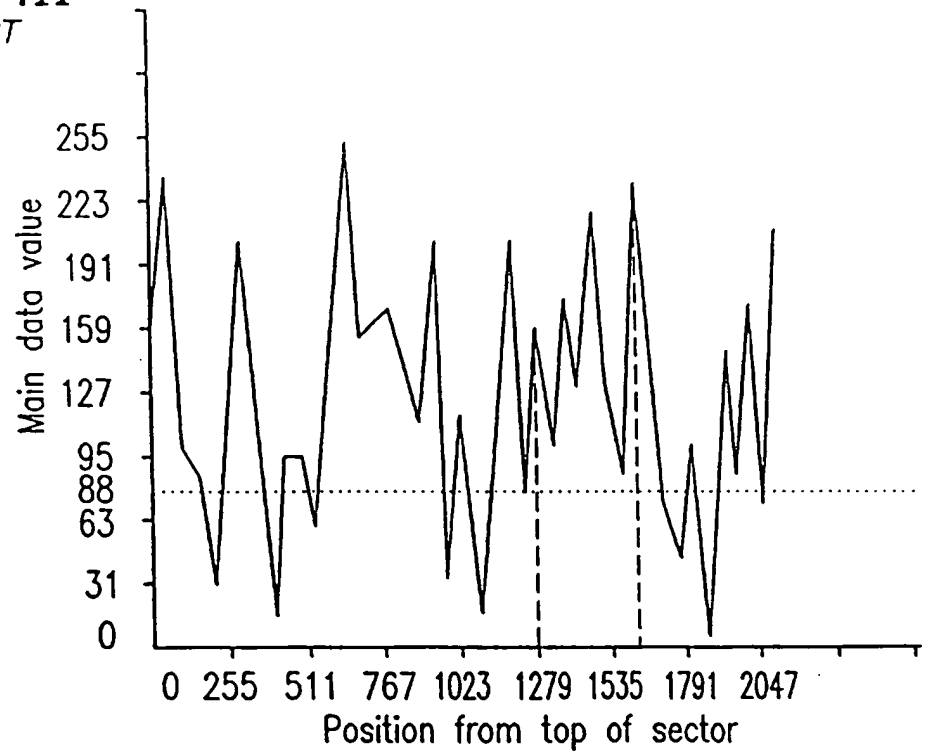
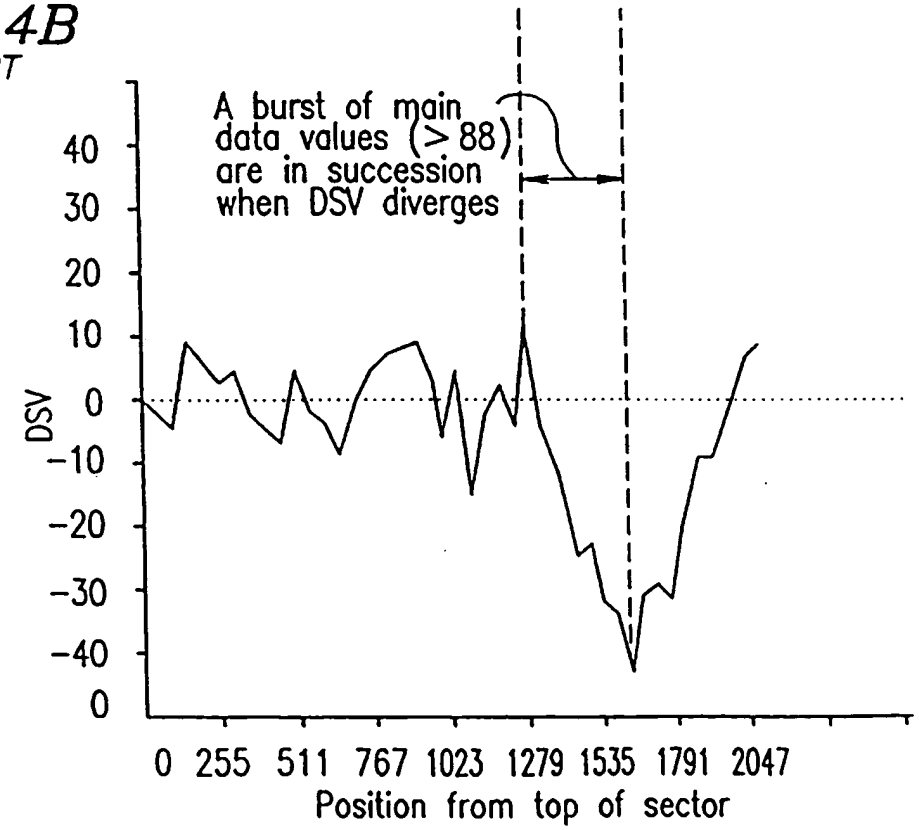



FIG. 24B
PRIOR ART